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Design and Implementation of DAC and Comparator using MOSFET

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***Abstract*— This paper focuses on designing and implementing a Digital-to-Analog Converter (DAC) and a comparator using MOSFETs in CMOS technology, with validation through Cadence Virtuoso simulations. The DAC converts digital binary inputs to precise analog signals using a modular approach involving inverters, AND gates, and a binary decoder to control a resistive ladder, ensuring high resolution and linearity. The comparator, built with CMOS differential amplifiers and inverters, compares two analog signals and outputs a binary result, with emphasis on speed, accuracy, and noise tolerance. Key performance metrics such as resolution, settling time, linearity (INL/DNL), and power consumption are analyzed through testbench simulations. The two components are integrated into a unified system to showcase their combined functionality. This scalable and efficient design approach delivers high precision and low power consumption, making it suitable for applications in signal processing, embedded systems, and VLSI designs.**

***Keywords*— MOSFET, ADC, DAC, Comparator, CMOS, VLSI.**

I. INTRODUCTION

Digital-to-Analog Converters (DACs) and comparators are crucial in modern electronics, bridging digital and analog domains for applications like audio playback, motor control, and medical monitoring. DACs convert digital signals into precise analog outputs, with types such as binary-weighted, R- 2R ladder, and sigma-delta DACs tailored for different performance needs. Comparators, in contrast, compare analog voltages and provide binary outputs, essential for decision- making circuits like Analog-to-Digital Converters (ADCs). As technology evolves, particularly in wearable devices, flexible electronics, and Internet of Things (IoT) applications, DACs and comparators must be optimized for low power consumption, miniaturization, and material flexibility.

To address existing challenges in designing efficient DACs and comparators for next-generation electronics, this project proposes a MOSFET-based 6-bit DAC with a folded resistive string structure and an OTA-based comparator. This approach ensures high accuracy, low power consumption, and compatibility with flexible and wearable substrates. By integrating these components into a unified ADC system, the design enhances signal processing efficiency while meeting the growing demands of healthcare, telecommunications, and consumer electronics.

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The project's innovations could drive advancements in AI-powered wearables, smart textiles, and energy-efficient IoT devices, shaping the future of low-power, flexible electronics.

In the literature survey, we studied various advancements in low-power and high-performance digital circuit design, focusing on magnitude comparators, digital-to-analog converters (DACs), and successive approximation register (SAR) analog-to-digital converters (ADCs). A two-bit magnitude comparator integrating Pass Transistor Logic (PTL), Transmission Gate Logic (TGL), and CMOS logic demonstrated improved power-delay efficiency for VLSI applications [1]. Similarly, a 4-bit R-2R DAC implemented in 45nm CMOS technology utilized a two-stage operational amplifier to enhance performance while minimizing power consumption and non-linearity errors [2]. Several SAR ADC designs were explored, including a 4-bit ring counter-based architecture for ultra-low power consumption [3], a 6-bit ADC with a split capacitor array for energy efficiency [4], and a 12- bit ADC in 65nm CMOS with enhanced robustness against process variations [5].

Furthermore, a hybrid Flash-SAR ADC in 28nm CMOS leveraged inverter-based comparators for improved energy efficiency [6], while a dynamic-controlled comparator in a SAR ADC at 45nm achieved ultra-low power consumption, making it ideal for biomedical and IoT applications [7]. Additional studies introduced high-precision CMOS comparators [8] and 12-bit SAR ADCs using FinFET technology, offering high-speed operation, low power consumption, and reduced non-linearity [9]. These advancements demonstrate significant progress in circuit design methodologies, utilizing novel architectures and optimization techniques to enhance energy efficiency, speed, and robustness in modern digital systems.

II. Objectives

A. Design of an OTA-based comparator

The OTA-based comparator is designed for low-power, high-efficiency analog signal comparison, essential for applications like ADCs and sensor-based systems. It efficiently amplifies small voltage differences while consuming less power than traditional designs, making it ideal for battery- operated devices such as wearable health monitors. By leveraging transconductance for fast binary switching, the comparator ensures real-time performance with optimized speed and energy efficiency. Its compact and scalable design makes it suitable for next-generation electronics, addressing the demands of flexible and portable systems.

B. Design of a 6-bit DAC

A Digital-to-Analog Converter (DAC) is a crucial component in modern electronics, converting digital signals into corresponding analog voltages. Among various DAC architectures, the resistive fold structure is recognized for its compact design and efficient resistor utilization. This structure employs a systematically folded resistor network to achieve digital-to-analog conversion while minimizing layout area and interconnect complexity. Unlike traditional resistor-based DACs, the resistive fold structure enhances performance by reducing parasitic effects and improving matching accuracy. This makes it highly suitable for applications requiring high resolution, low power consumption, and precise analog output, such as signal processing, embedded systems, and communication devices. By optimizing resistor placement and circuit symmetry, the resistive fold structure ensures reliable and efficient conversion, making it a valuable choice in precision-driven electronic systems.

III. Software Requirements

Cadence Virtuoso was utilized for the schematic design and simulation of both the DAC and comparator, providing a comprehensive environment for analyzing circuit performance. This industry-standard Electronic Design Automation (EDA) tool enables precise schematic capture, layout design, and simulation, ensuring accurate validation of analog and mixed- signal circuits. With its advanced simulation capabilities, Virtuoso allows for detailed analysis of key parameters such as power consumption, gain, linearity, and noise performance. The tool's compatibility with various CMOS technology nodes ensures reliable modeling of real-world circuit behavior, making it an ideal choice for optimizing the design and functionality of the DAC and comparator before fabrication.

IV. Methodology and Implementation

The design and implementation of the OTA-based comparator and 6-bit R-2R DAC followed a structured approach, beginning with circuit modeling and schematic design in Cadence Virtuoso. The OTA-based comparator was designed to achieve high precision and low power consumption, utilizing a differential input stage to enhance sensitivity and minimize offset errors. The R-2R DAC employed a resistor ladder network for

accurate digital-to- analog conversion, ensuring linearity and low power dissipation. We performed calculations on the obtained simulation results to evaluate performance metrics such as gain, resolution, power consumption, and speed.

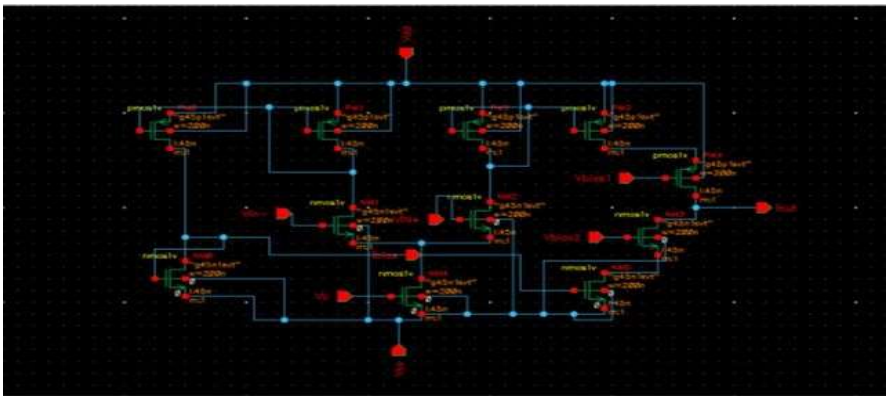

Fig.1. Comparator Design

A. Comparator design

The CMOS-based differential amplifier or comparator is a key component in analog signal processing, mixed-signal ICs, and analog-to-digital converters (ADCs), enabling accurate signal comparison in modern electronic systems. The design is optimized to meet several important performance requirements, ensuring compatibility with low-power systems and providing the necessary sensitivity and accuracy.

- Power Supply: The circuit operates with a supply voltage of 1.8V, typical for low-power, portable devices like wearable technology and IoT systems. This low voltage ensures energy efficiency while meeting the requirements of modern portable electronics.
- Input Voltage Range: The differential input pair must handle voltage swings that keep the NMOS transistors in the saturation region. This design choice ensures high gain and stable performance, crucial for accurate signal processing.
- Output Current: The output current, which represents the difference between input voltages, plays a vital role in converting small input variations into amplified output, enabling precise comparisons in mixed-signal applications.

The circuit aims to meet several design goals, including high sensitivity to small input differences, low offset voltage to minimize errors, and low power consumption to make it suitable for energy-efficient, low-power applications. Additionally, high-speed operation is crucial for fast-response applications such as real-time data processing and communication systems.

- Differential Input Stage: The core of the design consists of NMOS transistors (NM0 and NM1) configured as a differential pair. The width-to-length ratio of these transistors is chosen to achieve high transconductance, ensuring a fast response time and high gain for better sensitivity.
- Current Mirror: The PMOS transistors (PM0, PM1, PM2, PM3, PM4) form a current mirror, which ensures that the current flowing through the differential pair is mirrored and directed to the output stage. The current mirror increases the output impedance, thereby enhancing the gain of the circuit.
- Biasing Circuit: Precise biasing, controlled by voltages Vbias1 and Vbias2, is necessary for the proper operation of the circuit. These bias voltages stabilize the output stage and maintain consistent performance across process, voltage, and temperature variations.

The output current (Iout) directly reflects the difference in input voltages. When Vin+ > Vin-, the current through NM0 increases, shifting more current to the output, while if Vin+ < Vin-, the current through NM1 dominates, reducing the output current. This differential output current is critical for further stages, such as ADCs or amplification.

Presented below are the schematic diagram and its associated testbench for the design.

generation. This architecture is particularly advantageous for miniaturized and low-power applications, such as wearable electronics and IoT devices, due to its compact design and energy efficiency. By combining these elements, the resistive folding DAC achieves high accuracy and reliability, making it a suitable choice for modern electronic systems.

The design of the inverter consists of a PMOS transistor connected to VDD and an NMOS transistor connected to GND, with both transistor gates tied to the input and the output taken from their common drain. This CMOS inverter is a fundamental component in digital logic design, used for generating complementary signals. Its efficient configuration ensures that the output is always the logical complement of the input, making it essential for various digital and analog applications. Its simplicity, reliability, and low power consumption contribute to its widespread use in modern electronic circuits.

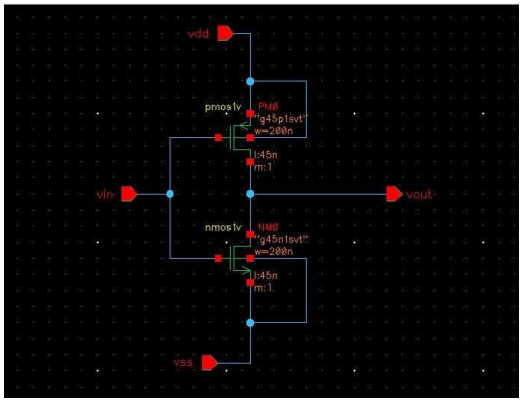

Fig. 3. Inverter schematic

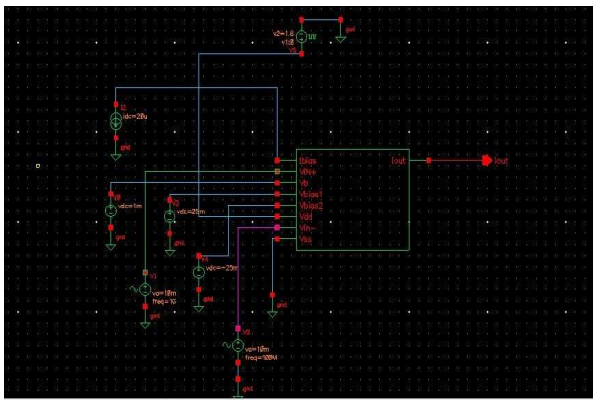

Fig. 2. Comparator testbench

AND gate is essential for controlling the selection of specific branches in the resistive DAC structure, ensuring precise digital-to-analog conversion. Its design utilizes CMOS transistors, with two NMOS transistors connected in series to implement the AND logic and two PMOS transistors arranged in parallel for proper pull-up functionality. The output is taken from the common drain of the PMOS and NMOS networks, ensuring reliable signal processing. This configuration provides an efficient balance of simplicity and performance, making it ideal for low-power and high-precision applications in modern electronic systems. The resistive folding Digital-to-Analog Converter (DAC) is an efficient architecture that translates digital signals into precise analog outputs using a resistor network for voltage division and binary-weighted inputs. Its design integrates several key components, including AND gates for binary control, inverters for generating complementary logic signals, decoders for selecting specific resistive branches, and a resistive ladder network for precise voltage generation. The AND gates ensure correct activation of the resistive branches, while inverters maintain signal integrity, particularly in high- speed applications. Decoders play a crucial role in mapping digital input values to corresponding voltage levels, and the resistive ladder network ensures accurate and linear output.

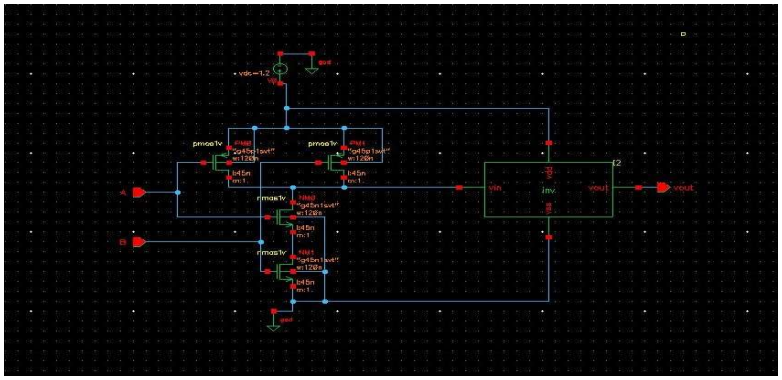

Fig. 4. AND schematic

The decoder is essential for enabling specific resistive branches in the DAC based on the binary digital input. It is designed using inverters to generate complementary signals and AND gates to combine these signals, ensuring that only one output line is activated per input code. In an N-bit DAC, the decoder has 2^N outputs, each linked to a resistor branch. Simulation involves applying all possible binary inputs to confirm that only one output is active (HIGH) at a time, guaranteeing accurate and reliable operation within the DAC architecture.

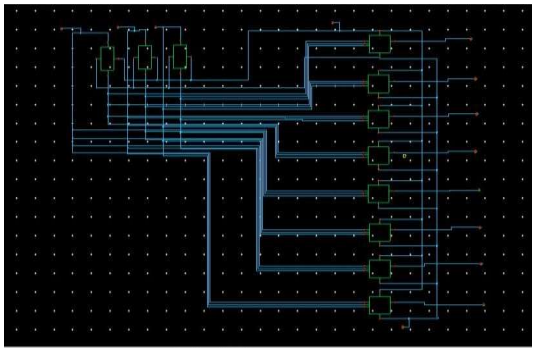

Fig. 5. 3:8 Decoder schematic

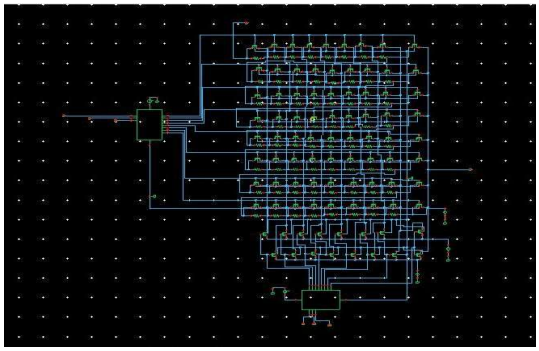

Fig. 6. DAC schematic

The resistive ladder network is a fundamental part of the DAC, converting digital signals into precise analog voltage levels through a structured voltage division from VDD to GND. It consists of equal-value resistors arranged in a folded configuration to ensure consistent voltage drops, with decoder outputs controlling NMOS switches that select specific nodes in the network. Resistor precision is crucial for accuracy, requiring careful matching to minimize systematic errors and parasitic effects. DC analysis is performed to verify that the output voltage aligns with expected analog values for each digital input. This compact and efficient design ensures high precision, making it ideal for modern low-power electronic systems.

After constructing the DAC circuit, a testbench is set up in Cadence Virtuoso to validate its functionality. This setup includes voltage sources representing binary inputs and measurement tools to analyze the DAC's output. Simulations assess key performance metrics such as resolution, linearity, settling time, and accuracy. The DAC network, consisting of NMOS-controlled switches, converts digital inputs into an analog output (Vout), ensuring correct proportional voltage generation. By analyzing simulation results, iterative optimizations are made to enhance power efficiency, speed, and precision, ensuring the DAC meets design requirements.

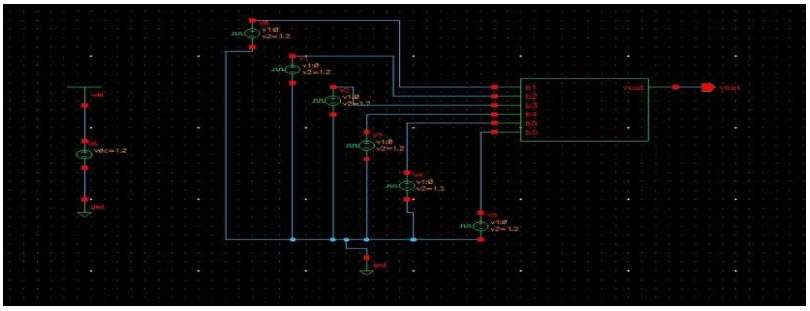

Fig. 7. DAC testbench

V. Results and Discussions

A. Comparator results

The simulation of the comparator circuit provides valuable insights into its performance under varying input conditions. The simulation includes three key waveforms: the output current (/iout), the input signal (/net3), and the reference signal (/net4), each playing a critical role in evaluating the behaviour of the comparator. The output current waveform exhibits sharp transitions between high and low states, reflecting the comparator's sensitivity to changes in the input signal. These abrupt changes occur in response to the varying relationship between the input and reference signals, showcasing the comparator's fast switching capability. This rapid response is essential in high-speed applications such as analog-to-digital converters or signal detection circuits, where quick and accurate decision-making is required.

The input signal, represented by the green waveform (/net3), is a high-frequency oscillating signal with small amplitude, simulating a low-level or noise-like input that fluctuates over time. This type of input allows the comparator's performance to be tested across multiple cycles, ensuring its ability to handle rapidly changing signals, which is typical in real-world applications. The reference signal, depicted by the magenta waveform (/net4), is a slower sinusoidal signal with a peak amplitude of around 500 mV, setting the threshold for

comparison. As the input signal crosses the reference signal's threshold, the output current sharply transitions, demonstrating the comparator's ability to accurately detect small variations in input signals and produce corresponding output states. This interaction validates the comparator's functionality, highlighting its effectiveness in precision applications where fast, accurate signal comparisons are critical.

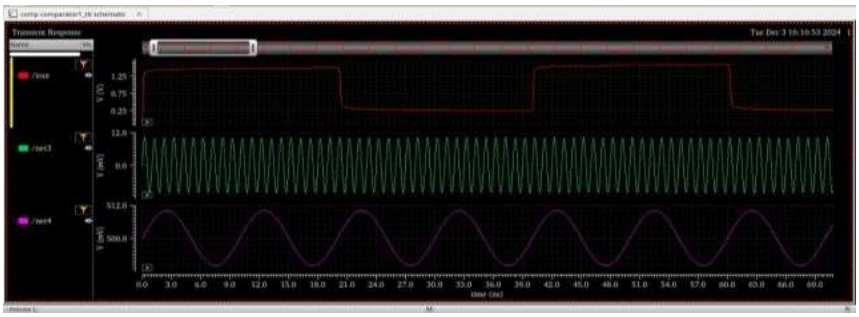

Fig. 8. Comparator simulation

The below table provides a detailed summary of the key performance parameters of a comparator circuit, which are essential for assessing its speed, stability, and overall efficiency. Each of these parameters provides crucial insights into the functionality and suitability of the comparator for specific applications, particularly those that require high-speed operation, precision, and reliability in signal processing.

TABLE I. COMPARATOR RESULTS

Parameter	Value
Rise time	2.934 ps
Fall time	108.7 ps
Propagation delay	55.817 ps
Settling time	480.6 ns
Slew rate	3.613 × 103 V/µs
Phase margin	180.0
Gain bandwidth product	34.86 × 10-15 Hz

B. DAC results

The transient response analysis of the DAC circuit provides critical insights into its efficiency, accuracy, and suitability for high-performance applications. The stepwise nature of the analog output confirms the expected 6-bit resolution, ensuring proportional voltage changes with each digital input increment, resulting in 64 discrete output levels. The synchronized input signals prevent glitches, enhancing output integrity and making the DAC reliable for real-time applications like video processing. The smooth waveform transitions and minimal distortion validate its ability to generate high-fidelity analog signals, crucial for audio playback and waveform synthesis. Additionally, the DAC demonstrates strong linearity, with minimal integral nonlinearity (INL), ensuring precision in applications requiring accurate digital-to-analog conversion. These results confirm the DAC's robustness and reliability, making it well- suited for advanced electronic systems.

Fig. 9. DAC simulation

The DAC results table provides a comprehensive evaluation of the circuit's speed and accuracy through key performance metrics, including rise time, fall time, propagation delay, and linearity measures such as integral non-linearity (INL) and differential non-linearity (DNL). The DAC demonstrates high-speed performance, with a rise time of 513.0 ps and a fall time of 486.7 ps, ensuring rapid signal transitions. Its low propagation delay of 499.85 ps minimizes latency, making it suitable for real-time applications. The exceptionally low INL (0.533 LSB) and DNL (0.497 LSB) values confirm excellent linearity and step size uniformity, ensuring precise signal conversion without glitches. These characteristics make the DAC ideal for high-speed communication, instrumentation, audio processing, and other advanced electronic systems requiring both speed and precision.

TABLE II. DAC RESULTS

Parameter	Value
Rise time	513.0 ps
Fall time	486.7 ps
Propagation delay	499.8 ps
INL	0.533 LSB
DNL	0.497 LSB
Resolution	6 bits

VI. ACKNOWLEDGMENT

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