

Comparative Analysis of CMOS Phase Frequency Detector

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Abstract—This manuscript presents the various design of almost significant electronic circuit used in modern wireless systems, known as Phase frequency detector. The phase-frequency detector is widely utilized in Phase-Locked-Loop (PLL) circuits, and its characteristics significantly affect PLL performance. In this work, different design topologies of PFD have been studied and evaluated their performance in terms of operating frequency, power dissipation, dead band, jitter and blind band.

Index Terms— power dissipation, phase noise, jitter, dead zone, frequency.

I. INTRODUCTION

In the last two decades, much attention has been given to clock generation, recovery, synchronization, and distribution [1-2]. In high-speed clock alignment applications, the PLL and the delay locked-loop (DLL) are the two automated control approaches that are most often used [3]. The PLL and DLL circuits' main component is the phase-frequency detector (PFD) [4]. This feature has caused the phase detector's significance in high-speed communication systems to increase. The phase detectors have been classified into combinational phase detectors, time to voltage converters and sequential phase detectors based on their characteristics. The combinational phase detector (XOR) has a dead zone issue and enables to detect the little phase difference between the rising/falling edges of the REF and BACK signals [5–6]. Due to this problem, the phase-locked loop locks in an incorrect phase. The PFD circuit generates a very narrow pulse in the up or down direction, when differences between input signals are very small, is known as a dead zone. The charge pump misses such small pulses, leaving the LPF with no current injection—a situation that is essentially analogous to having no phase difference. The jitter will occur at the output, and the PFD sensitivity is affected [7-9] due to this dead band problem. The dead zone can be eliminated in the PLL System using the following methods.

- a) Extending the PFD reset route [10–11] with an adequate delay to make it longer than the charge pumps current switching time.
- b) For a brief period, activating the UP and DOWN signals simultaneously may swiftly activate the charge pump switches [12–13].

The time-to-digital converter may be used for phase detection (TDC). In this instance, to calculate the delay between reference and received signal a digital counter is used. The TDC-based phase detectors have higher hardware complexity compared with combinational phase detectors. Sequential PFD is commonly employed in the PLL circuits, mainly in frequency-synthesizers. Digital circuits may be used to build sequential PFDs, which operate with binary input waveforms. As a result, they are acknowledged as digital PFD. The greater input range of the sequential PFD allows for an increase in locking speed and acquisition range [14]. Designing of a low-

power, high-speed phase detector that works well across an extensive frequency range is a design challenge.

II. PHASE FREQUENCY DETECTOR'S DESIGN ISSUES

A PFDs performance is affected by the following critical factors: dead zone, blind zone, power dissipation, operating frequency, and duty cycle variations. The brief descriptions of these design issues are

- **Dead-Zone:** Ideally, the PFD has zero dead-zone. In practically it arises when the phase difference between the input pulses is closer to 0° , then PFD produced an output signal with a very narrow width. The small width of the UP and DOWN signal has not enabled switching ON and OFF charging and discharging switches of the charge pump. This makes improper discharging and charging of filter. For the efficient design of PFD, the value of the dead-zone should be small.
- **Blind-Zone:** Blind-Zone: The PFD's frequency insensitivity to some change in the input signals is known as blind-zone. The blind zone occurred when the PFD kept phase difference between two input signals is close to $\pm\pi$. It limits the PFD's detection range and deteriorates the locking characteristics of PLL.
- **Maximal operating frequency ($f_{\max}$):** It is the extensive range of frequency at which PFD can operate steadily. The $f_{\max}$ of the PFD can be expressed as [15]

$$f_{\max} = \frac{1}{2 \times \Delta T_R}$$

where ΔT_R is the reset delay time of the PFD. The operating frequency of PFD can be increased by decreasing the reset delay time.

- **Power-Dissipation:** Power dissipation is the primary concern in PFD design. The large power dissipation is inevitable in high-frequency operations.

III. RELATED RESEARCH

The main design challenges in PFD circuits are obtaining a high operating frequency, minimum power dissipation, and minimization of the dead-band and blind-band. In the last two decades, designers have been reported numerous design techniques [16-51] to improve these essential parameters. A standard design of combinational phase detectors is a Gilbert cell is presented [16-17] as shown figure 3.1. The Gilbert cell operates as an analog multiplier when a small amplitude signal is utilized to its input. Analog multiplier works non-linearly and has a tracking-range of $-\pi/2$ to $\pi/2$. It has the advantage of high speed of operation but suffers from large static power dissipation and occupies large area. On the other hand, the Gilbert cell behaves as an XOR gate when a large amplitude signal is applied to its input. The XOR phase detector improves the acquisition range from 0 to π , but its disadvantage is that the input signals' duty cycle is not considered.

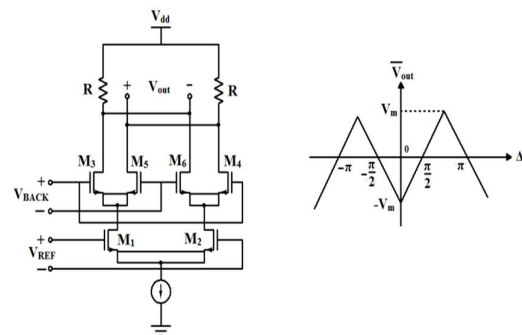


Figure 3.1: Gilbert cell phase detector

In [18-19], S. Soliman presented an edge-triggered phase detector based on the RS latch, as shown in figure 3.2. The advantages of the RS latch phase detector are improved acquisition range from 0 to 2π . However, RS latch suffers from many drawbacks (i) Clock and data recovery circuits using an RS latch PD cannot be done frequency-synthesis because the frequency at the output is similar to inputs. (ii) Because of the meta-stability that develops in the lock state, output jitter persists.

S. Li et al. reported the PFD with the tri-state techniques [20-21] to detect input signals' phase and frequency difference. Figure 3.3 illustrate the tri-state PFD which composed of a couple of D flip-flops with their inputs attached to supply voltage, i.e., high logic and one AND gate. The tri-state PFD has an advantage of improved

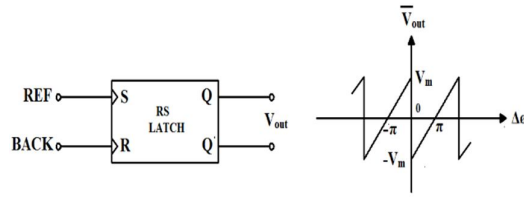


Figure 3.2: RS latch phase detector

lock speed and acquisition range. On the other hand, it includes the demerits of the non-zero dead band, the existence of jitter, large power dissipation, and consumes a large area.

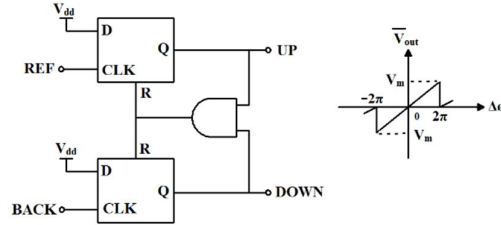


Figure 3.3: Tri-state PFD

In [22], H. O. Johansson introduced a pre charge CMOS PFD to decrease the jitter-noise and the problem of the dead band. The PFD circuit is simple has no feedback, as shown in figure 3.4, utilizing 18 transistors. The detector was simulated in 0.8 μm CMOS technology and operates at 800 MHz frequency. This PFD obtained no dead-band and is essential in low-jitter communication products.

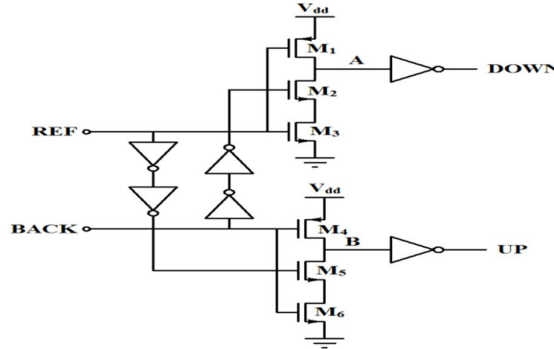


Figure 3.4: Precharge PFD

Further, T. Johnson reported the improved architecture of tri-state PFD [23] to enhance the phase-detection range (PDR). The figure 3.3 illustrated the modified dynamic logic PFD circuit. The design included the advantages of no dead band in its characteristics, minimum blind band, and high operating frequency, but it suffers from a large power dissipation of 10 mW.

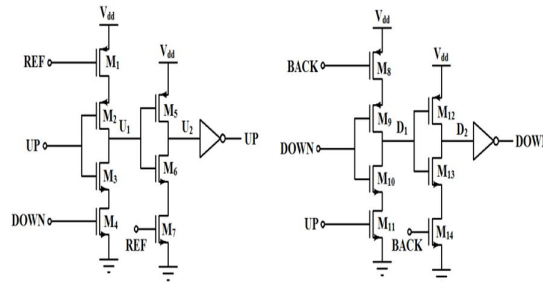


Figure 3.5: Improved architecture of tri-state PFD

The non-sequential linear CMOS PFD is proposed in [24-25] for the application of high-speed clock generation and data recovery circuits. The structure of non-sequential PFD is depicted in figure 3.6. The designed PFD eliminates the metastable-state by dropping the D-flip flop. The advantage of PFD is that it exhibits linear phase characteristics and obtains a high operating speed of up to 10 Gbits/s.

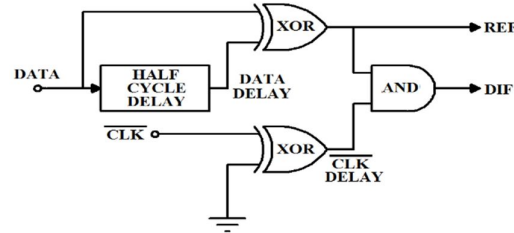


Figure 3.6: Non-sequential PFD

N. M. H. is mail et al. suggested the falling edge PFD [26] for low power applications. The FE-PFD is depicted in figure 3.7 which is designed at 0.18 μ m technology to remove the dead band problem, and dissipates less power of 6.6 μ W working at the clock frequency of 50MHz but it has drawback of low operating frequency. The PFD exhibits the noise of -168.8 dBc/Hz.

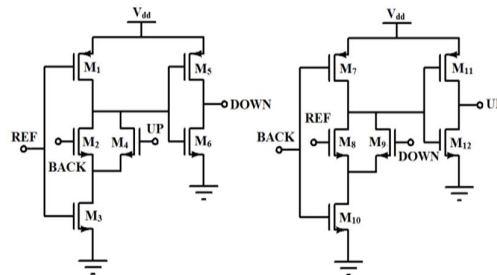


Figure 3.7: Falling edge PFD

In [27], W. H. Chen et al. reported a method to eliminate the blind zone, which is brought on by the internal nodes' pre-charge time. With this method, the pre-charge time is cut in half, and PFD obtained a tiny blind-band. However, the PFD's reset mechanism produces a blind-zone that hinders quick PLL acquisition by lowering the input detection range, reducing the PFD gain, and exacerbating the cycle-slip effect. The PFD showed in figure 3.8 is designed in 0.13 μ m process, including advantage of the smaller blind zone of 61 ps but the drawback of lower operating frequency.

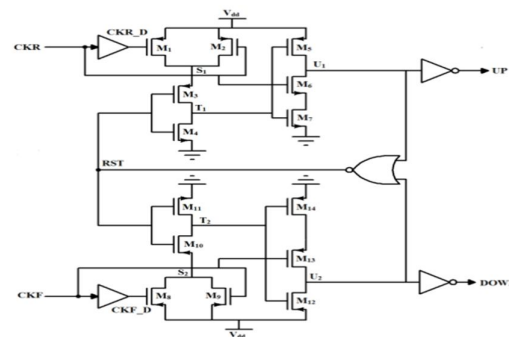


Figure 3.8: Modified PFD with additional M_2

To eliminate the reset path, an improved design of PFD has been reported in [28-29]. The reset path has been removed by adding the pass transistor logic (PTL), minimizing the blind-zone and accelerating acquisition. The PFD design is shown in figure 3.9. The designed PFD has been constructed by the use of 10 transistors, has the advantages of reducing the area and power consumption of 73% and 99 %, respectively, compared with conventional design [30-33]. However, the demerit of this design is poor phase noise performance. Further, M.

Gholami suggested a new design to reduce the reset path and improve operating frequency [34]. Figure 3.10 shows the PFD design, which comprises a total of 14 transistors. The merits of the designed PFD circuit include low power dissipation of 134 μ W, low rest path of 80 ps, less number of transistors used, and there is no constraint of 50% duty cycle for the input signal suffers from blind band problem.

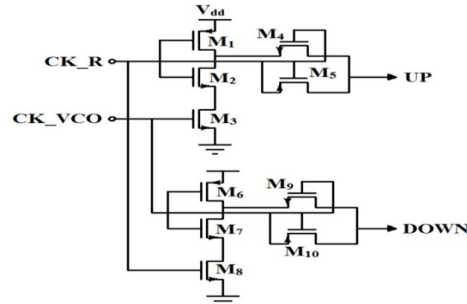


Figure 3.9: PFD with PTL and M9 transistors

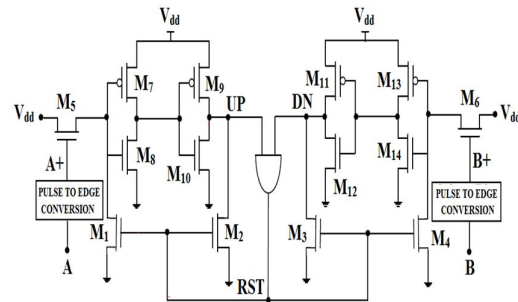


Figure 3.10: PFD circuit with low reset path

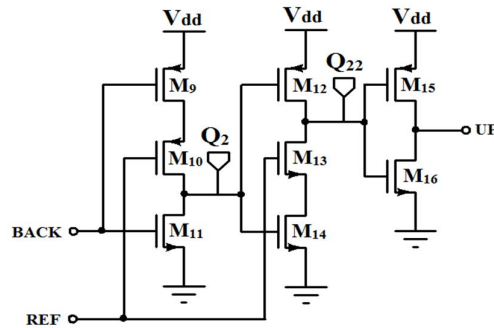


Figure 3.11: Pre-charge PFD circuit (a) Down block

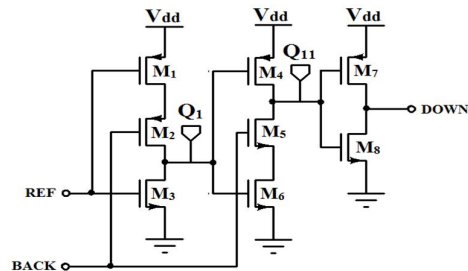


Figure 3.11: Pre-charge PFD circuit (b) UP block

For lowpower dissipationPD circuits, G. Nikolic et al. suggested the precharged PFD circuit in [35–39]. The precharge PFD design is implemented with 16 transistors, as illustrated in figure3.11, comprises two identical

blocks with no feedback. It contains two stages called p-precharge and n-precharge; they have been linked together in a cascade configuration and are driven by an inverter that generates the signal DOWN and UP. The merit of this design includes the low power dissipation of 0.412 mW at 1GHz, high operating frequency up to 8 GHz, but it has a drawback of blind band problem.

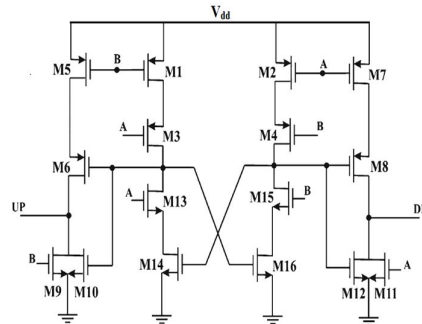


Figure 3.12: PFD with positive feedback

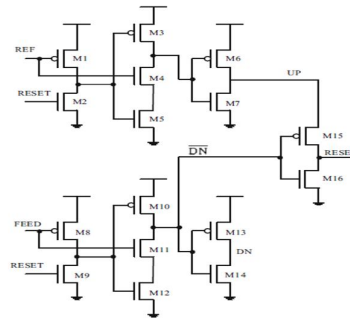


Figure 3.13: PFD based on a AND gate and D flip-flop

S. Sofimowlodi et al. [40-45] presented the PFD structure with two positive feedback is shown in figure 3.12. The positive feedback eliminate the dead band and increase the working frequency of PFD but it has drawback of instability if positive feedback loop gain is less than unity. The PFD has been simulated with TSMC 0.13 μm technology achieved low power dissipation and dead band when operating at 4.1 GHz frequency. Further, A. Rezaeian et al. [46-51] presented a new structure of PFD that utilized AND-gate in GDI logic and a couple of D flip-flops in TSPC logic. The reported PFD has been designed with 16 transistors to achieve low power of 110 μW , and enables the PFD to operate at a higher frequency of 3.33 GHz.

IV. CONCLUSION

Due to the vital role of PLL systems in modern applications, such as wireless communications, high-speed data processors, etc., extensive research is going in this field in recent years. Hence the research on PFD has been selected to enhance the overall PLL performance. Various topologies of PFDs have been explored based on different parameters. There are some advantages and demerits which are associated with each designed PFDs. The important parameters in designing PFDs are dead band, operating frequency range, power dissipation, and area. These design parameters will be taken care of while designing the proposed detector circuits to achieve the desired performance.

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