

A Class AB Current Controlled Second Generation Voltage Conveyor using Self Cascode Current Mirror

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Abstract—A current controlled second generation voltage conveyor circuit implemented using self-cascode current mirrors with enhanced performance has been proposed in this paper. The proposed circuit is based on class-AB technique which is employed at the input and output stages. Proposed circuit provides high linearity, large bandwidth and negligible offsets. Parasitic impedances at terminals Y and Z of the proposed voltage conveyor circuit can be independently controlled by dc bias currents. This feature can be fruitfully utilized in the realization of different electronically tunable analog circuits, and also to reduce the use of external resistors. The functionality of the circuit is verified by simulation using 180nm CMOS technology and supply voltage of $\pm 0.9V$.

Index Terms— Second generation voltage conveyor, Self-cascode current mirror, CMOS analog circuits.

I. INTRODUCTION

Conveyors are used to convey current or voltage signals from one port to other ports. These can be used as an important analog building block to design circuits with improved characteristics. The concept of current conveying and its implementation as current conveyor was introduced in [1]. Current conveyors, particularly CCII [2], take advantage of current mode signal processing to obtain better linearity, more accuracy, improved frequency performance and simpler circuits when compared with op amps. However, in applications where voltage output is required, an extra CCII block arranged as voltage buffer, will be required to be connected at the output for impedance matching. Voltage conveyor as dual of current conveyor was introduced in [3]. A Current buffer forms its input stage and output stage is a voltage buffer as opposed to CCII where input and output stages are interchanged. Low output impedance of voltage follower stage of VCII makes it advantageous to be used in analog circuit designs requiring voltage output. This also provides saving in terms of chip area and power consumption when compared with similar circuit realizations using CCII. VCII offers simplified methodology for designing analog systems with current or voltage output and also presents new solutions to applications where use of CCII is limited [4]. Multiple analog circuit implementations viz. various filters, grounded inductor, rectifier, capacitance multiplier, resistor-less $\pm C$ simulator, employing VCII can be found in [15-23]. Many CMOS realizations of second generation voltage conveyors have been reported in the literature [4-

10]. Electronic tunability of VCII parasitics is not considered in the implementations reported in [4-7] and [10]. Voltage controlled second generation voltage conveyor (VC-VCII) as dual of current controlled second generation current conveyor (CCCII) is proposed in [8]. In this parasitic resistance at terminal Z is controlled by a dc bias voltage, but parasitic resistance at terminal Y is controlled by varying the supply voltage for current follower stage. Therefore, for perfect tunability of the parasitic at Y, this supply voltage should not be affected by internal resistance of the circuit. This necessitates use of extra voltage buffer stage. Power consumption of the proposed circuits is also very large in [8]. Voltage controlled VCII is also proposed in [9], however it offers electronic tunability of parasitic resistance at Y only.

In this work a current controlled VCII (CVCII) circuit is proposed where parasitic impedance at terminals Y and Z can be independently controlled using dc bias currents I_{B1} and I_{B2} respectively. To support low-voltage low-power operation along with enhanced characteristics as compared to conventional cascode current mirror, circuit employs self-cascode current mirrors. Both input and output stages are operating as class-AB to enhance linearity and bandwidth, consume low power and give negligible dc offsets. The paper is organized as follows: A brief review on VCII is given in section II. In section III proposed circuit is presented along with small discussion on self-cascode current mirror. Section IV provides the simulation results using 180nm CMOS technology and comparison of performance parameters with some previous relevant works, while section V concludes the paper.

II. VCII BRIEF REVIEW

Internal structure and electrical symbol of VCII without parasitic impedances are given in Fig. 1.

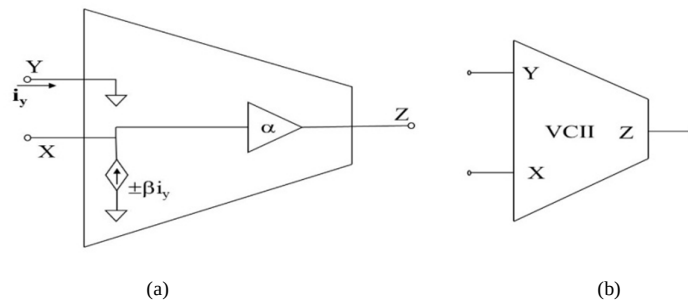


Figure 1. VCII (a) Internal structure (b) Electrical symbol

Three terminals of VCII are X, Y and Z. It has current follower as the input stage between Y and X, output stage is a voltage follower between X and Z. Impedance seen at Y and Z terminals is ideally zero while at X it should be infinite. Its characteristics equations can be given by the following matrix:

$$\begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \pm\beta & 0 & 0 \\ 0 & \alpha & 0 \end{bmatrix} \begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix}. \quad (1)$$

where ' β ' and ' α ' denotes current gain and voltage gain respectively; $+\beta$ indicating $VCII^+$ and $-\beta$ is for $VCII^-$. Ideally ' β ' and ' α ' should be unity.

The schematic diagram of non-ideal VCII with parasitic impedances at low frequencies is given in Fig. 2 [8]. In this r_x and r_z represent the output impedances at terminals X and Z while r_y is input impedance at terminal Y. Parasitic impedances observed are due to transconductances and output impedances of the transistors.

It can be modelled by following matrix (including non-ideal characteristics):

$$\begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} = \begin{bmatrix} r_y & 0 & 0 \\ \pm\beta & \frac{1}{r_x} & 0 \\ 0 & \alpha & r_z \end{bmatrix} \begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix}. \quad (2)$$

III. PROPOSED CIRCUIT

The proposed voltage conveyor circuit employs self-cascode current mirrors to achieve better performance and low voltage operation.

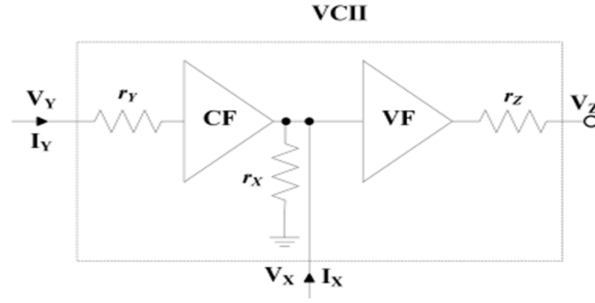


Figure 2. VCII schematic with parasitic resistance [8]

A. Self-Cascode Current Mirror

Current mirrors employed in a circuit are expected to have high output impedance, decent accuracy of current transfer, low input voltage and low minimum output voltage [12]. However, due to channel length modulation effect there is always some scope of improvement in achieving these properties for various current mirrors. The normal cascode current mirror structure attains higher gain and output impedance as it suppresses the channel length modulation effect, but its output signal swing—a deciding factor for dynamic range of the circuit—is limited, and that can then be improved by using self-cascode structure [13-14].

A method of designing composite field effect transistor by series parallel association of single transistors was given in [11]. Composite transistor offers high transconductance to output conductance ratio similar to long channel transistor. Fig. 3(a) shows a self-cascode structure consisting of series association of two transistors with gate terminal being common to both. Aspect ratio of cascode transistor M_2 is kept 'm' times that of driver transistor M_1 for achieving optimal operation ($m > 1$).

For the structure shown in Fig. 3(a), to function properly, transistor M_1 should be working in linear region while M_2 can be in linear or saturation region where M_1 acts as resistor (R_{ON}) and M_2 acts as resistor or current source with its value depending on the gate bias voltage [13]. These operating conditions for M_1 and M_2 also leads to a voltage difference between source and drain of M_1 so small that there is no apparent V_{DSAT} difference between composite and simple transistors. Thus, self-cascode structure is well suited for low voltage operation. Equations characterizing the overall effective β (β_{eff}), effective transconductance (g_{meff}) and output resistance into drain (r_{oeff}) of the composite structure can be given as [13]:

$$\beta_{eff} = \frac{\beta_1 \beta_2}{\beta_1 + \beta_2} = \frac{m}{m+n} \beta_1 \approx \beta_1, \quad (3)$$

$$g_{meff} = g_{m1} \sqrt{\frac{m}{m+n}} \approx g_{m1}, \quad (4)$$

$$r_{oeff} = R_{ON1} + [1 + (g_{m2} + g_{mb2}) R_{ON1}] r_{o2}, \quad (5)$$

where $n = 1 + (g_{mbx}/g_{mx})$ and other symbols have their usual meaning. Also, $R_{ON1} = 1/g_{m1}$ i.e., resistance of M_1 working in the linear region is same as its transconductance in saturation being inverted, and it is input dependent too.

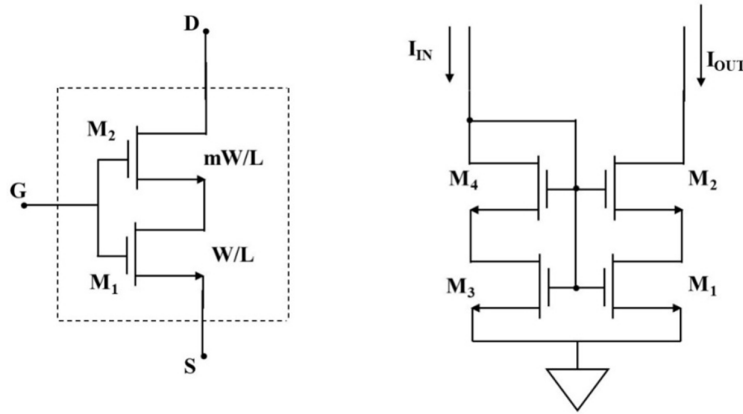


Figure 3. (a) Self-cascode composite NMOS transistor (b) Self-cascode current mirror

Current mirror implemented utilizing the self-cascode structure to obtain improved output swing and high output impedance, is shown in Fig. 3(b). Aspect ratios for M_3 and M_4 are perfectly matched to that of M_1 and M_2 respectively. Desired optimal operation of circuit is established when aspect ratios for the cascode transistors (M_2 , M_4) are chosen to be much higher than that of driver transistors (M_1 , M_3). This self-cascode current mirror structure has been used to realize all current mirrors that are part of the VCII architecture proposed in this work.

B. Proposed VCII Circuit

Fig. 4 shows the proposed voltage conveyor circuit. Transistors M_1 - M_4 and M_5 - M_8 are used to implement class-AB operation for both current follower and voltage follower stages.

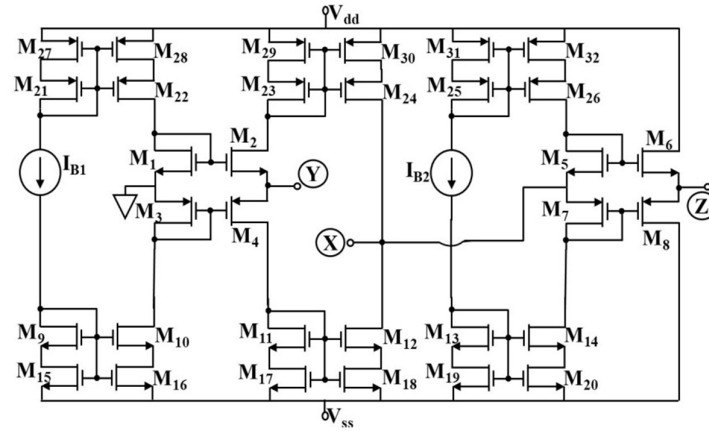


Figure 4. Proposed VCII circuit

All other transistors, M_9 - M_{32} , are constituting different self-cascode current mirrors used in the circuit. Two current sources I_{B1} and I_{B2} bias the input and output stages of VCII independently. This circuit architecture results in wide bandwidths even for low bias currents.

For the current buffer stage, I_{B1} mirrored through M_1 and M_3 generates gate bias voltage. I_{B2} does the same for voltage buffer stage. Current to input terminal Y is copied to terminal X by self-cascode current mirrors. Voltage at terminal X is buffered to terminal Z.

For g_{m2} , g_{m4} , g_{m6} and g_{m8} being transconductance parameters of M_2 , M_4 , M_6 and M_8 respectively, resistance at Y and Z terminals can be given as:

$$R_Y \approx \frac{1}{g_{m2} + g_{m4}} = \frac{1}{\sqrt{2\beta_2 I_{B1}} + \sqrt{2\beta_4 I_{B1}}}, \quad (6)$$

$$R_Z \approx \frac{1}{g_{m6} + g_{m8}} = \frac{1}{\sqrt{2\beta_6 I_{B2}} + \sqrt{2\beta_8 I_{B2}}}. \quad (7)$$

where $\beta_{2,6} = \mu_n C_{ox} (W/L)_{2,6}$ and $\beta_{4,8} = \mu_p C_{ox} (W/L)_{4,8}$.

Both R_Y and R_Z can be controlled independently by bias currents I_{B1} and I_{B2} respectively. Therefore operation of the circuit as current controlled VCII is possible. Also, resistance at terminal X can be approximately given by the following expression:

$$R_X \approx r_{oeffa} \parallel r_{oeffb} \parallel r_{oeffc} \parallel r_{oeffd}. \quad (8)$$

where r_{oeffa} , r_{oeffb} , r_{oeffc} and r_{oeffd} are the effective output resistances of self cascode current mirrors consisting of transistors (M_{11} , M_{12} , M_{17} and M_{18}), (M_{23} , M_{24} , M_{29} and M_{30}), (M_{13} , M_{14} , M_{19} and M_{20}) and (M_{25} , M_{26} , M_{31} and M_{32}) respectively. The output conductance and transconductance of the self-cascode structures will also vary when the bias currents are varied. Output resistances of self-cascode currents mirrors will therefore also vary and hence affecting R_X as well.

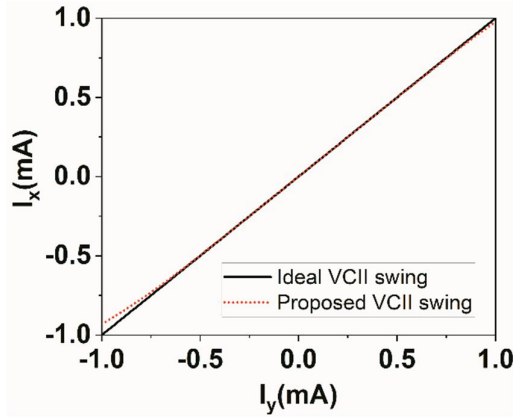
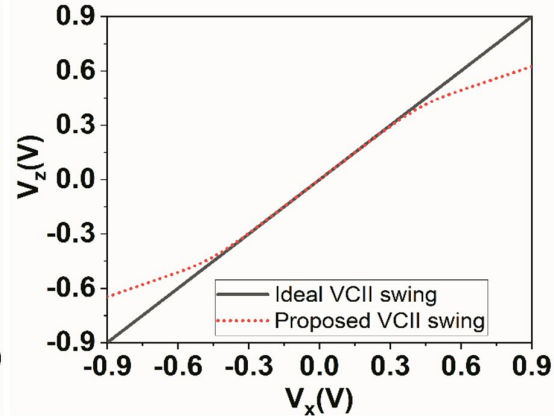
IV. SIMULATION RESULTS

The proposed VCII circuit has been simulated using standard 180nm CMOS technology at supply voltage of $\pm 0.9V$. Both the bias current sources have been taken to be of value $20\mu A$ each. Aspect ratios used in simulation for all the transistors are given in table I.

TABLE I. TRANSISTORS ASPECT RATIO

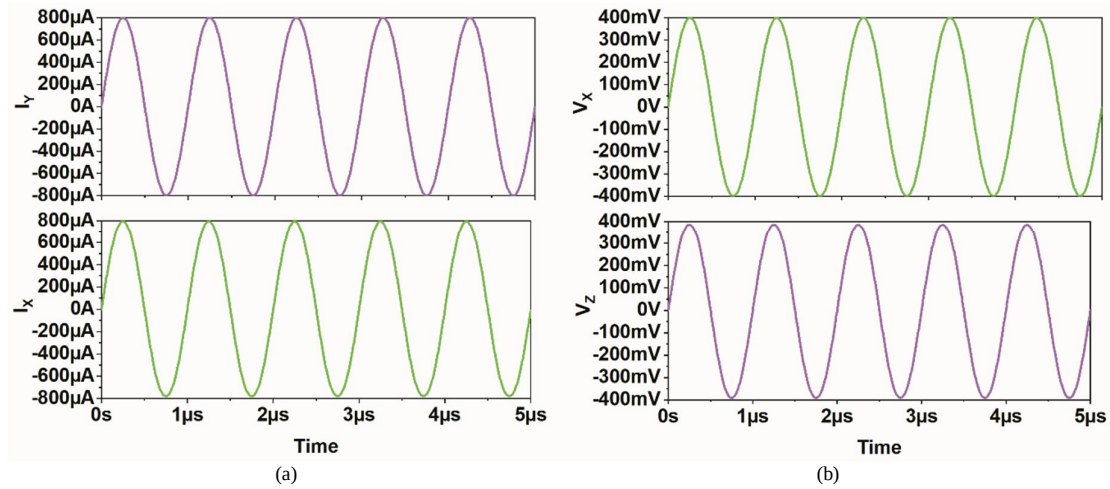
Transistor	W/L Ratio	Type
M ₁ , M ₂	3/0.3	NMOS
M ₃ , M ₄	10/0.3	PMOS
M ₅ , M ₆	30/0.3	NMOS
M ₇ , M ₈	90/0.3	PMOS
M ₉ -M ₁₄	20/0.3	NMOS
M ₁₅ -M ₂₀	5/0.6	NMOS
M ₂₁ -M ₂₆	60/0.3	PMOS
M ₂₇ -M ₃₂	15/0.6	PMOS

DC characteristics of the proposed VCII circuit are plotted for both the current buffer and voltage buffer stages, as shown in Fig. 5 and Fig. 6 respectively. Current input to terminal Y is varied from -1mA to 1mA. Range of DC current observed at X is from -800 μ A to 1mA.

Figure 5. Current I_x vs current I_y Figure 6. Voltage V_z vs voltage V_x

For voltage buffer, range of -400mV to 400mV is seen when voltage input to it is varied from -0.9V to 0.9V. Error is about 3.4% at -800 μ A end of the extreme for current buffer, and about 5% at 400mV for the voltage buffer.

Transient performance of the circuit is investigated by applying sinusoidal inputs. Figs. 7(a) and 7(b) depicts the same. Current linearity is checked by peak current of 800 μ A at 1MHz applied to Y. THD for current at X is 0.84% with 1 Ω connected to X. For voltage buffer performance analysis sinusoid of peak 400mV at 1MHz is applied to X. With no load at terminal Z, THD value observed is 0.82% for V_z .

Figure 7. Transient response (a) I_x vs I_y , (b) V_z vs V_x

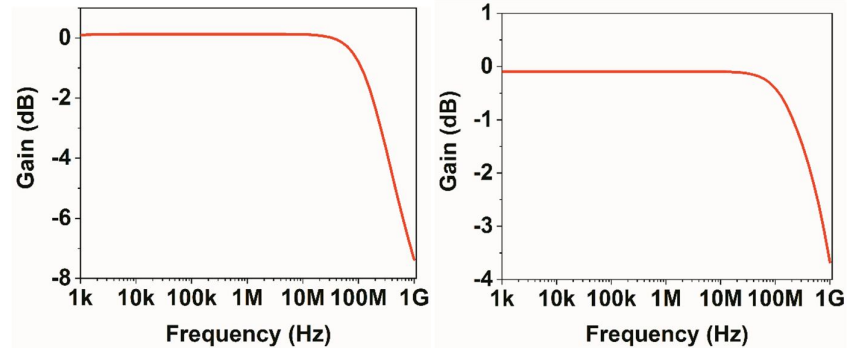


Figure 8. Frequency response: Current gain Figure 9. Frequency response: Voltage gain

Figs. 8 and 9 show ac characteristics of the proposed architecture. Current gain (β) and voltage gain (α) observed are 1.01 and 0.989 with corresponding bandwidths of 241.69MHz and 780.60MHz respectively. Impedance at Y (R_Y) varies from 4.26k Ω to 896 Ω as dc bias current I_{B1} is changed from 5 μ A to 80 μ A. Variation of current I_{B1} will also disturb impedance at X (R_X). Fig. 10 and Fig. 11 depict the variation of R_Y , and R_X (with $I_{B2}=20\mu$ A), when I_{B1} is altered in steps of 5 μ A. Similarly, results for impedance at Z (R_Z) is displayed in Fig. 12 for I_{B2} varying from 5 μ A to 100 μ A through steps of 10 μ A. Value of R_Z is observed to be changing from 2.39k Ω to 213.48 Ω . Corresponding change in R_X is shown in Fig. 13 with I_{B1} kept at 20 μ A.

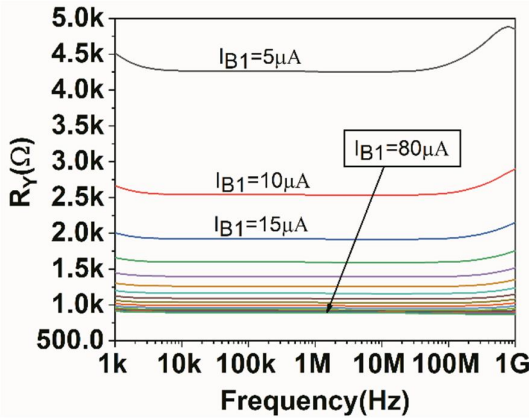


Figure 10. I_{B1} variation effect on R_Y

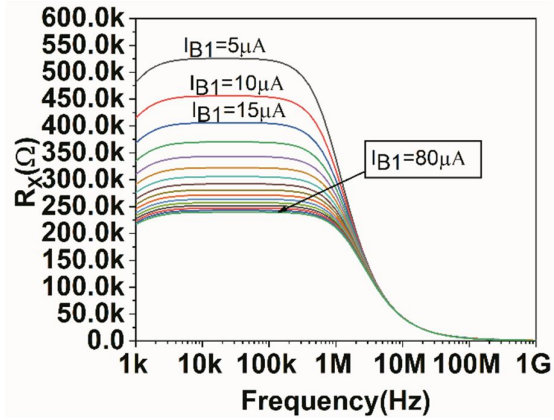


Figure 11. I_{B1} variation effect on R_X

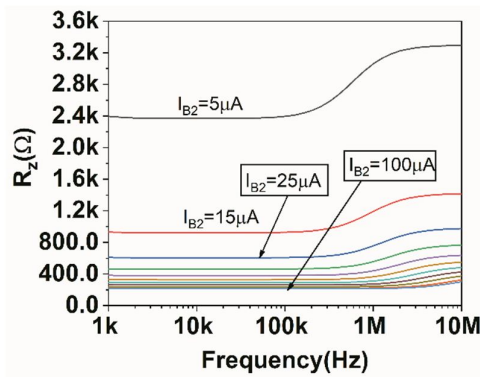


Figure 12. I_{B2} variation effect on R_Z

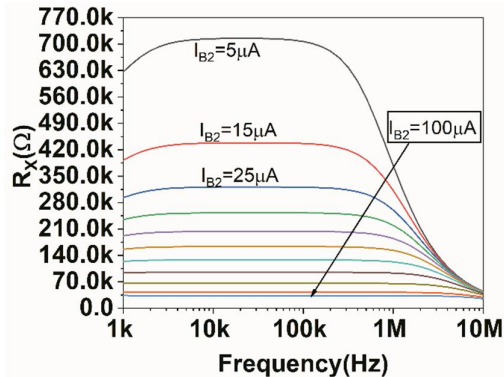


Figure 13. I_{B2} variation effect on R_X

Table II summarizes different performance parameters of the proposed VCII and comparison with some previous works. The proposed circuit achieves good linearity range, wide bandwidth and near ideal gains. From the references presented in the table, electronic tunability feature is considered in [8]a and [8]b only. However, as

seen, these consume much higher power when compared with the proposed VCII. Also, improvements in terms of offsets, harmonic distortion and noise performance are observed for the proposed VCII with respect to other works.

TABLE II. PERFORMANCE SUMMARY OF PROPOSED VCII AND COMPARISON WITH OTHER WORKS

Parameter	This work	[6]	[5]	[8]a	[8]b	[10]
Technology	0.18 μ m	0.15 μ m	0.18 μ m	0.18 μ m	0.18 μ m	0.35 μ m
Supply voltage	± 0.9 V	± 0.9 V	± 0.9 V	± 0.9 V	± 0.9 V	± 0.9 V
Class	AB	AB	AB	A	A	AB
Current gain (β)	1.01 @100kHz	-0.03dB @100kHz	1.0	0.988	0.988	0.1dB
Voltage gain (α)	0.989 @100kHz	-0.24dB @100kHz	0.987	0.968	1	-0.02dB
Current gain BW	241.69MHz	165MHz	169.7MHz	794MHz	794MHz	71MHz
Voltage gain BW	780.60MHz	55MHz	100GHz	2.57GHz	1.92GHz	3.2MHz
Power consumption	253.39 μ W	120 μ W	179 μ W	664 μ W	622 μ W	28 μ W
Offset current	0.12 μ A	NA	NA	0.43 μ A	0.43 μ A	NA
Offset voltage	0.52mV @100kHz	NA @100MHz	-80.48mV	612mV	-0.9mV	NA
R_Y R_X R_Z	1.59k Ω 369.21k Ω 729.54 Ω	23 Ω 522k Ω 160 Ω	1.88k Ω 273.8k Ω 1.75k Ω	930 Ω 74.28k Ω 705 Ω	930 Ω 74.28k Ω 35 Ω	160 Ω 1.9M Ω 367 Ω
THD at I_X	0.84% ($I_Y=1.6$ mA _{p-p} @1MHz)	1.1% ($I_Y=1$ mA _{p-p} @1MHz)	1% ($I_Y=2.44$ mA _{p-p} @1MHz)	NA	NA	-51dB
THD at V_Z	0.82% ($V_X=0.8$ V _{p-p} @1MHz)	2.4% ($V_X=1.6$ V _{p-p} @1MHz)	1% ($V_X=1.78$ V _{p-p} @1MHz)	NA	NA	-50.8dB
IRN current at Y IRN voltage at X	@10MHz 4.63 pA/ $\sqrt{Hz}$ 5.27 nV/ $\sqrt{Hz}$	NA NA	NA NA	@10MHz 7.16 pA/ $\sqrt{Hz}$ 4.53 nV/ $\sqrt{Hz}$	@10MHz 7.16 pA/ $\sqrt{Hz}$ 20.16 nV/ $\sqrt{Hz}$	@1kHz 130pA/ $\sqrt{Hz}$ 182nV/ $\sqrt{Hz}$

V. CONCLUSION

Current controlled VCII presented in this paper can be used to design various electronically tunable low-voltage analog circuits. Variation of parasitic resistances with dc bias current has been investigated. This feature can also be used to reduce the use of external resistances. The proposed circuit takes the advantage of self-cascode current mirror and class-AB stages to achieve good linearity, large bandwidth and negligible offsets while operating at low voltage of ± 0.9 V.

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