Grenze International Journal of Engineering and Technology, January Issue

Five Level Modified CHB Inverter with Switch Level Redundancy

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***Abstract*— Multilevel inverters have become increasingly important in medium to high power applications due to their ability to produce high-quality output voltage with reduced harmonic distortion and lower electromagnetic interference. Among the various multilevel inverter topologies, the cascaded H-bridge (CHB) inverter stands out for its modularity, scalability and potential for fault tolerance. This paper presents a five-level modified CHB (MCHB) inverter topology incorporating redundancy to enhance reliability, fault tolerance and power quality. A device level redundancy is deployed for fault tolerance against open switch fault. For identification of faults, RMS and average value of output voltage of inverter is measured continuously and compared with threshold levels. MATLAB simulation results are presented to demonstrate the fault tolerant operation with redundancy. The system was observed to respond to the fault and restore normalcy within single cycle.**

***Index Terms*— Multilevel Inverter, Fault Detection, Redundancy, voltage sensing.**

I. INTRODUCTION

The five-level modified cascaded H-bridge (CHB) inverter represents an advanced class of multilevel inverter that synthesizes an AC output with five distinct voltage levels. This configuration yields a superior approximation of a sinusoidal waveform and lower total harmonic distortion than conventional two-level inverters [1]. A principal benefit of this modified topology is its decreased requirement for power switches relative to a conventional CHB inverter of equivalent output level. This streamlined design offers advantages in cost, physical size, and overall system efficiency [2]. Although it retains the modular architecture fundamental to CHB inverters, the five-level output is achieved through an innovative arrangement of H-bridge units and supplementary switching elements. A notable trade-off for this component reduction is the potential for more complex control algorithms and heightened electrical stress on the individual switches [3]. Nevertheless, these inverters are increasingly applied in renewable energy integration, motor drive systems, and industrial automation, where their enhanced waveform quality and economic benefits are highly valued [4].

Within contemporary power electronics, multilevel inverters (MLIs) are critical for generating high-fidelity voltage waveforms by combining several DC voltage steps [5]. A significant threat to their reliability is the open-switch fault, a condition where power semiconductors (e.g., IGBTs, MOSFETs) become inoperative due to factors like thermal stress, aging, or gate driver failure. These faults induce output waveform distortion, generate damaging harmonics, and can precipitate total system breakdown if not promptly addressed [6].

Grenze ID: 01.GIJET.12.1.516_1

Therefore, implementing effective fault detection is essential for maintaining operational stability and reducing downtime in MLI-dependent systems [7].
The manifestation of an open-switch fault includes recognizable signatures such as absent voltage levels, asymmetrical phase currents, and, in specific topologies like diode-clamped or flying capacitor designs, capacitor voltage imbalances [8]. These irregularities degrade power quality and place additional stress on functional components, highlighting the necessity for rapid fault identification. Conventional detection strategies frequently employ analyses of voltage and current waveforms. Techniques like the Fast Fourier Transform (FFT) pinpoint harmonic anomalies, while algorithms that check for waveform symmetry or missing levels can map distortions to particular faulty switches [9]. More direct methods involve monitoring switch voltages during conduction periods or cross-referencing gate signals with anticipated states to provide localized diagnostic data [10].
Advanced detection frameworks incorporate model-based approaches, such as state observers and parity equations, which compare real-time system behavior against mathematical models to produce residual signals indicating faults. Signal processing tools like wavelet transforms and Park's Vector Analysis further refine detection by capturing transient features or revealing imbalances in the dq0 reference frame [11, 12]. In cascaded H-bridge MLIs, specialized strategies monitor the output of each cell to isolate faults. Concurrently, artificial intelligence (AI) methodologies, including neural networks and fuzzy logic classifiers, are being developed to identify fault patterns with high precision using historical or simulation-derived data [13, 14, 15, 16].
Recent research trends have focused on minimizing the component count in multilevel inverters to reduce their cost, size, and control complexity. This has spurred the proposal of numerous modified CHB topologies. However, even with these architectural simplifications, switch faults remain a prevalent issue, making their detection a critical research objective. This paper investigates a voltage-sensing-based fault detection method for a five-level modified CHB inverter and presents supporting MATLAB simulation results for fault identification and redundancy at switch level.

II. Fault Detection and Redundancy Controller for Five Level MCHB Inverter

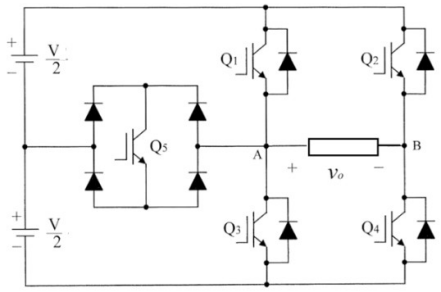

Figure 1: Five Level Modified CHB Inverter Topology

The circuit configuration of a five level modified CHB inverter is shown in Figure 1. The modified inverter topology utilizes only five IGBT switches, a significant reduction from the eight required in a conventional five-level Cascaded H-Bridge (CHB) design. The circuit is powered by two series-connected DC sources, each with a value of V/2. Switches Q1, Q2, Q3, and Q4 are configured in a standard H-bridge arrangement, while an auxiliary switch, Q5, is connected at the node common to Q1 and Q3.
This configuration generates five distinct output voltage levels: +V, +V/2, 0, -V/2, and -V. The specific switching states to achieve these levels are detailed in Table 1. For instance, an output of +V is produced by activating switches Q1 and Q5. Similarly, the +V/2 level is achieved by turning on Q4 and Q5, while the zero-voltage level can be generated by conducting either the pair Q3 and Q4 or Q1 and Q2.
The output voltage equation of the sine wave inverter is given as,

$$V_O = V_m \sin(\omega t) \quad \ldots (1)$$

The mean value of the output voltage is calculated as are under the curve as,

$$V_{mean} = \int V_O \quad \ldots (2)$$

$$V_{mean} = \int V_M \sin(\omega t) \quad \ldots (3)$$

With all devices in healthy state, the equation 3 is evaluated to be 0

$$V_{mean} = 0 \quad \ldots (4)$$

The RMS value is evaluated by taking integration of square root of the squared terms over one cycle. Therefore, the RMS value is,

$$V_{RMS} = \int \sqrt{{V_O}^2} \quad \ldots (5)$$

With all switching devices in healthy state, equation 5 is evaluated as

$$V_{RMS} = \frac{V_M}{\sqrt{2}} \quad \ldots (6)$$

Hence when inverter's switching devices are in healthy state, the mean and average values of the measured output voltage shall be strictly in accordance with equation 4 and equation 6. On the basis of average and RMS voltage measurement, redundancy controller is developed as seen in figure 2

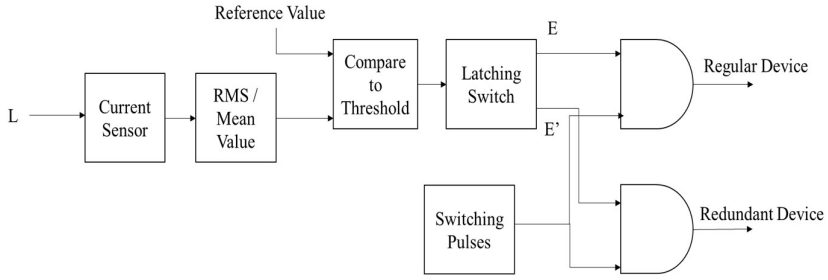

Figure 2: Fault Detection and Redundancy controller

III. MATLAB SIMULATION AND RESULTS

The specifications of MATLAB Model are mentioned in table 1 and the MATLAB Simulink Model is seen in figure 3. The Simulink model consists of three main elements. The main element being five level modified CHB inverter. In this inverter, every switching device is connected with parallel redundant switching device and hence device level redundancy is configured.

TABLE I: SYSTEM SPECIFICATION

Inverter	Single phase Five level Modified CHB
Switching device	IGBT
Output Voltage	230V
Frequency	50HZ
Load	Resistive (2kW)
Fault detection	Voltage sensing
Technique	Measurement of average and RMS value
Redundancy	Switch level

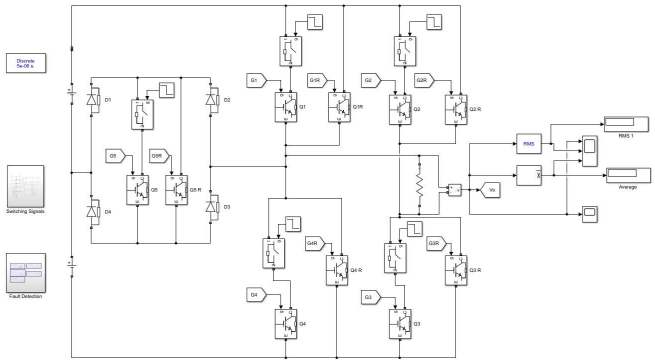

Figure 3 MATLAB Model of Five Level MCHB Inverter with Redundancy

The simulation model is executed for 0.6 seconds and the switching devices Q1, Q2, Q3, AQ4 and Q5 are subjected to fault at time instances 0.1 second, 0.2 second, 0.3 second, 0.4 second and 0.5 second respectively. Upon occurrence of fault, the fault detection logic for the individual IGBT generates fault flag and the gate pulses of regular IGBT are transferred to the redundant IGBT and thereby continuous inverter output is obtained. The graph of instantaneous output of inverter, average value and RMS value is shown in figure 4.

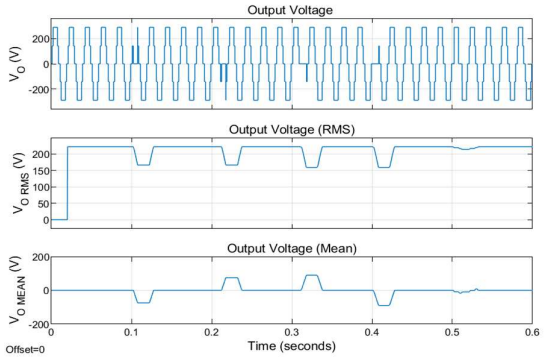

Figure 4 Inverter output voltage, Average value and RMS Value

The deviation in mean and RMS value of the inverter output voltage triggers the fault detection logic and redundancy controller to switch the gate pulses from regular device to the redundant device. The waveforms of fault flags of all the IGBTs is seen in figure 5 The waveforms of gate pulses of all the regular and redundant IGBTs is shown in figure 6. The redundancy controller responds to all the faults within single cycle and restores the inverter to normalcy. The inverter output voltage waveforms are seen in figure 7.

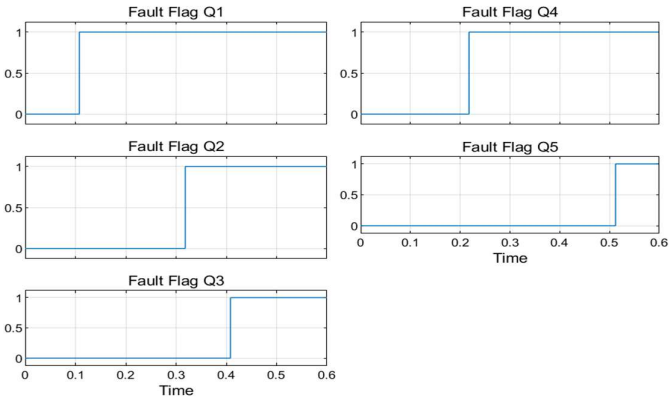

Figure 5 fault signals of IGBTs

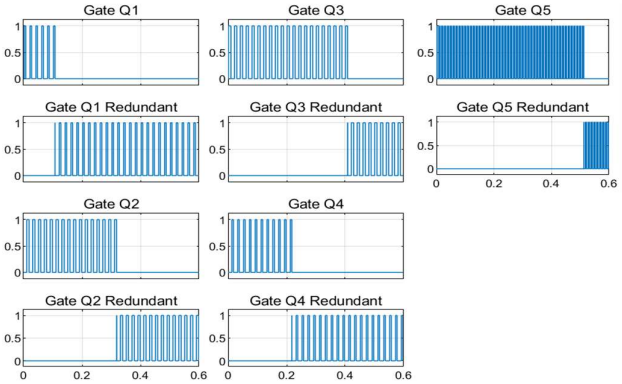

Figure 6 Gate Pulses of regular and redundant switching devices

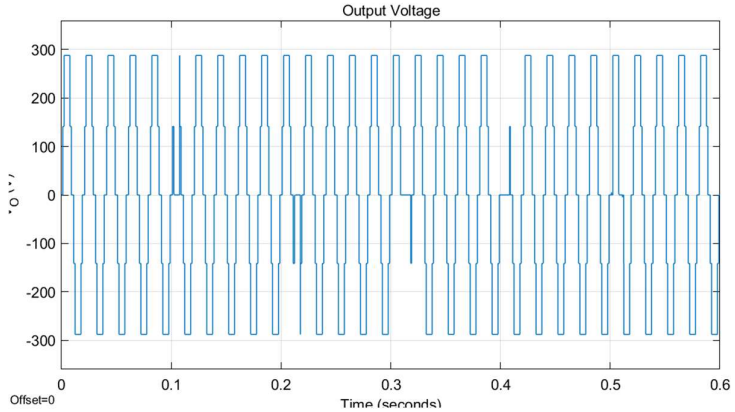

Figure 7 Inverter Output Voltage Waveforms

The simulation model illustrates robust fault-tolerant operation. When a switch or cell experiences an open-circuit fault, redundant switching paths automatically engage, allowing the inverter to maintain a symmetric and balanced output even under failure conditions. This self-healing capability is crucial for critical loads in ensuring uninterrupted delivery of rated power and voltage. The waveforms clearly shows that the redundancy controller is capable of switching the redundancy device by stopping regular one in case of fault and the inverter operation is restored within single cycle.

V. CONCLUSIONS

The simulation and experimental results of the five-level modified cascaded H-bridge (CHB) inverter with redundancy demonstrate significant improvements in reliability and fault tolerance. Analysis shows that the stepped output waveform remains uniform throughout the inverter operation with regular as well as redundant switching device in operation. The open switch fault in either of the IGBT of inverter detected and stable operation of the inverter is restored within single cycle of inverter output voltage.

ACKNOWLEDGMENT

The authors wish to thank Department of Electrical Engineering, PVPIT, Budhagaon for their support throughout this work.

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